Aarfa Bano Sheikh

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EDUCATION

North Carolina State University, Raleigh, NC — Aug 2024 – May 2026
Master of Science in Computer Engineering — **GPA: 3.61/4**
Coursework: ASIC/FPGA Design, ASIC Verification, Advanced Verification with UVM, Microprocessor Architecture, Architecture of Parallel Computers, Advanced Computer Architecture: Data Parallel Processors (GPGPU), Neural Networks

MKSSS's Cummins College of Engineering for Women, Pune, India — Aug 2016 – May 2020
Bachelor of Technology in Electronics & Telecommunication Engineering — **GPA: 9.08/10**

SKILLS

Programming Languages: C, C++, Verilog, SystemVerilog, Python, Tcl, CUDA C++
ASIC Design Tools: Synopsys Design Compiler, Mentor Graphics, Xcelium, Vivado, MATLAB
Architecture & Protocols: RISC-V, GPGPU, Cache Coherence (MESI/MOESI), AMBA (APB/AHB/AXI), PCIe, I2C, UART, Ethernet
Other Tools & Platforms: Linux/Unix, Git, Docker, VS Code, Jupyter, Jira, Jenkins, Tableau, Minitab, Jama, Perforce

WORK EXPERIENCE

Front-End CAD Engineer (Co-op), Skyworks Solutions, Inc., San Jose, USA — **Jun 2025 – Dec 2025**
- Accelerated SoC verification cycles through CAD automation and scripting, streamlining simulation setup and data analysis
- Automated regression flows using custom-built data wrappers, improving consistency in test execution and report analysis
- Built UVMF tests for timing modules using YAML-driven interfaces and transaction modeling to enable functional coverage
- Integrated Jenkins-based job scheduling to streamline nightly regressions and enable scalable verification workflows
- Improved mixed-signal verification by integrating log-based error detection and coverage tracking into CAD flows, and enabled Questa VIQ adoption through coverage analysis, training, and flow integration for verification teams

Electrical Engineer II, Baxter Innovations & Business Solutions Pvt. Ltd., Bengaluru, India — **Sept 2020 – Jul 2024**
- Drove component engineering and board-level redesign to extend medical device lifespan by 10+ years, leading qualification, verification, and reliability testing to ensure performance and cost optimization in high-reliability environments
- Migrated designs from Altera to Microchip and Xilinx, ensuring full functionality through timing, power, and thermal analysis
- Designed a high-performance valve driver on Xilinx Spartan-6 FPGA with Verilog HDL for delivering noise-free operation

R&D Intern, Knorr-Bremse Technology Center India Pvt. Ltd., Pune, India — **May 2019 – Jul 2019**
- Enhanced microcontroller communication reliability by developing and validating Low-Level Drivers for Infineon's Aurix TC233 Microcontroller, leveraging C programming, I2C, SPI, and UART protocols

PROJECTS

High-Performance Floating-Point Matrix Multiplier with MAC and SRAM Integration (Verilog)
- Designed a floating-point matrix multiplier with SRAM-based storage and optimized FSM-based control and data path management using DesignWare MAC module
- Simulated and synthesized the logic design in ModelSim and Synopsys DC, ensuring functionality and performance-area efficiency

Hardware Accelerator for Scaled Dot-Product Attention in Transformer Architectures (Verilog)
- Designed a fully synthesizable Verilog-based hardware accelerator for Scaled Dot-Product Attention in Transformer models, featuring a 28-state FSM for efficient matrix operations and parallel memory access with multiple SRAM interfaces
- Achieved optimal performance-area efficiency through detailed timing analysis and debugging on Visualizer

Cache and Memory Hierarchy Simulator (C++)
- Developed a cache and memory hierarchy simulator implementing LRU replacement and write-back write-allocate policies
- Designed a prefetch unit with multiple stream buffers, utilizing LRU policy and issued miss rates and memory traffic analysis

Out-of-Order Superscalar Processor Simulator (C++)
- Developed a cycle-accurate simulator for an out-of-order superscalar processor with configurable pipeline stages, dynamic scheduling, variable instruction latencies, and performance analysis to optimize pipeline instruction flow and bottlenecks

GPU Cache Optimization and Bypassing in GPGPU-Sim (C++)
- Developed profiling-based L1 cache bypass in GPGPU-Sim by tracking SM/kernel memory accesses to optimize cache usage
- Optimized SM load/store logic to bypass L1 cache using runtime profiling, improving IPC on cache-unfriendly benchmarks
- Evaluated LRU & FIFO policies across L1/L2 caches under varied SM configurations to analyze performance and miss trends

Scalable 3D FFT Implementation using OpenMP and Thread Optimization (C++)
- Built 3D Fast Fourier Transform using OpenMP parallel programming model to improve computational efficiency
- Achieved significant execution time reduction through thread scaling and scheduling mode optimization

Functional Verification of I2C Multiple Bus Controller (SystemVerilog)
- Designed a layered testbench architecture to verify the I2C Multiple Bus Controller (I2CMB) supporting both Wishbone and I2C protocols, including randomized stimulus and structured read/write sequences; simulated on Questa